REMARKS/ARGUMENTS

This Amendment is in response to the Final Office Action mailed June 11, 2008 and the Advisory Action dated August 27, 2008. Claims 1-70 were pending in the present application and are rejected.

Applicant has amended claims 1, 17, 18, 19, 20, 23, 24, 26, and 46. Claims 48-70 have been canceled claims without prejudice. Applicant submits that no new subject matter has been introduced by the amendments. Claims 1-47 remain pending in this application after entry of this amendment.

Reconsideration of the rejections is requested in view of the remarks below.

THE CLAIMS

Cancellation of multiple claims

Applicant has canceled several claims (48-70) without prejudice to reduce the total number of pending claims and to focus the prosecution of this application. The claims have not been deleted for reasons of patentability. Applicant reserves the right to reintroduce the canceled claims in this or continuing applications.

Rejections under 35 U.S.C. 103

Claims 1-15, 18, 20-44, 46-48, 50-62 and 64-70

Claims 1-15, 18, 20-44, 46-48, 50-62 and 64-70 are rejected under 35 U.S.C. §103(a) as being unpatentable over Maher, III et al (U.S. Patent No. 6,654,373) (hereinafter "Maher") in view of Scholten (U.S. Patent No. 7,126,956) (hereinafter "Scholten"). Applicant respectfully traverses the rejections.

Claim 1

Applicant submits that claim 1 is not taught or suggested by Maher or Scholten, considered individually or in combination. Applicant submits that there are several reasons why claim 1 is not taught or suggested by a combination of Maher and Scholten.

For example, Applicant's claim 1 specifically recites:

> 1. A circuit for aggregating a plurality of input data streams from first processors into one data stream for a second processor, said circuit comprising:
>
> . . .
>
> an aggregation module coupled to said plurality of ingress data ports and configured to receive the plurality of input data streams from the first processor using the plurality of ingress data ports, wherein an input data stream from a first processor is received via the ingress data port coupled to the first processor, said aggregation module adapted to analyze and combine the plurality of input data streams into one aggregated data stream . . . ;
>
> a memory coupled to said aggregation module, said memory adapted to store analyzed data packets; and
>
> an output data port coupled to said aggregation module, said output data port adapted to output the aggregated data stream to the second processor. (Applicant's claim 1, in part, emphasis added)

Claim 1 recites a circuit for aggregating a plurality of input data streams from first processors into one data stream for a second processor. As recited in claim 1, circuit includes an aggregation module that receives several input data streams from a plurality of ingress data ports. Accordingly, the aggregation module receives multiple input streams from a plurality of input ports. Claim 1 specifically recites that the aggregation module receives an input data stream from a first processor via the ingress data port coupled to the first processor. The aggregation module further analyzes and combines the plurality of input data streams into one aggregated data stream, which is then output to a second processor via an output data port coupled to the aggregation module. A memory is also coupled to the aggregation module for storing the analyzed data packets.

Applicant submits that an aggregation module, as recited in claim 1 is not taught by Maher or Scholten. The Final Office Action asserts that several of the elements of claim 1, including the aggregation module, are taught by Maher. More specifically, the Final Office Action asserts that the aggregation module recited in claim 1 is taught by reference 140 in Fig. 2 of Maher. Applicant respectfully disagrees.

As described above, claim 1 specifically recites that the aggregation module is coupled to a plurality of ingress data ports and receives multiple input data streams from the first processors via the plurality of ingress data ports, wherein an input data stream from a first processor is received via the ingress data port coupled to the first processor. Applicant submits that this is not done by reference 140 depicted in Fig. 2 of Maher. Reference 140 in Fig. 2 of Maher refers to a traffic flow scanning processor that receives data over a single fast-path bus 126 from PHY interface 102 (Maher: Fig. 2 and col. 6 lines 11-14). Accordingly, the traffic flow scanning processor 140 in Maher receives a single data stream via a single bus from PHY interface 102. This is different from claim 1, which specifically recites that the aggregation module receives a plurality of data streams and is coupled to a plurality of ingress data ports, each ingress port coupled to a corresponding first processor.

Applicant would also like to note that, while the single data stream received by traffic flow scanning processor 140 in Maher may contain data received over multiple ports of network apparatus 100 depicted in Maher Fig. 2, the traffic flow scanning processor 140 itself is not coupled to multiple input data ports and does not receive multiple input data streams, as recited in claim 1. Accordingly, Applicant submits that reference 140 depicted in Fig. 2 of Maher does not teach or anticipate the aggregation module recited in claim 1.

In the Advisory Action, the Examiner asserted that:

> Applicant argues that Fig. 2, 140 of Maher does not teach aggregation module that receives data streams from plurality of ports and combines them. However, examiner disagrees. Col. 6 lines 5-14 teach Fig. 2, 102 can consists of plurality of ports. Therefore, if plurality of ports are sending data to 140 aggregation module combines these data stream and analyzes then in Payload Analyzer. (Advisory Action)

It appears from the above that the Examiner has misunderstood how references 102 and 104 in Maher work and interact. Col. 6 lines 5-14 of Maher describe that physical interface 102 comprises a plurality of ports and can accept a number of network speeds and protocols, i.e., physical interface 102 comprises a plurality of ports for receiving data – not for sending data to module 140, as asserted in the Advisory Action.

Further, col. 6 lines 5-14 describe that physical interface 102 takes the data from the physical ports, frames the data, and then formats the data for placement on fast-path data bus 126 which is preferably an industry standard bus. Accordingly, contrary to what the Advisory Action asserts, Maher clearly indicates that data is communicated from physical interface 102 to module 140 over a single bus. Module 140 thus receives a data stream from physical interface 120 over a single bus. Thus, even though physical interface 120 comprises a plurality of ports, this does not teach or imply that module 140 (which the Examiner has compared to the aggregation module recited in claim 1) is connected to a plurality of data ports or receives a plurality of data streams, as recited in claim 1.

Based upon the above, Applicant submits that an aggregation module, as recited in claim 1, is not taught or suggested by Maher.

Additionally, the circuit recited in claim 1 comprises a specific structure. For example, claim 1 recites:

> 1. (Currently Amended) A circuit for aggregating a plurality of input data streams from first processors into one data stream for a second processor, said circuit comprising:
>
> a plurality of ingress data ports, each said ingress data port coupled to a corresponding first processor and adapted to receive an input data stream from the corresponding first processor, . . .;
>
> an aggregation module coupled to said plurality of ingress data ports and configured to receive the plurality of input data streams from the first processors using the plurality of ingress data ports, wherein an input data stream from a first processor is received via the ingress data port coupled to the first processor, . . . ;
>
> a memory coupled to said aggregation module, . . .; and
>
> an output data port coupled to said aggregation module, said output data port adapted to output the aggregated data stream to the second processor. (Applicant's claim 1, in part)

As recited above, claim 1 recites a specific structure. Applicant submits that such a structure is not taught or suggested by Maher or Scholten.

With respect to the specific structure recited in claim 1, the Final Office Action acknowledges that

> . . . Maher does not teach [that] each data port is coupled to a corresponding processor and receives data from its corresponding processor, and an aggregating module receives the input data streams from the first processors using the plurality of ingress data ports. (Final Office Action: page 5).

The Final Office Action however goes on to assert that

> Scholten teach each data port is coupled to a corresponding processor and receives data from its corresponding processor, and an aggregation module receives the input data streams from the first processors using the plurality of ingress data ports **[Col. 7, lines 47-49]** (Final Office Action: page 5)

Applicant respectfully disagrees. As discussed above, Applicant submits that an aggregation module as recited in claim 1 is not taught by Maher. Applicant submits that the deficiencies of Maher are not cured by Scholten. Scholten thus fails to teach or suggest an aggregation module as recited in claim 1. Consequently, the specific structure recited in claim 1 of an aggregation module coupled to a plurality of ingress data ports and receiving multiple data streams from the input ports and each ingress data port coupled to a corresponding first processor and adapted to receive an input data stream from the corresponding processor is also not taught or suggested by Scholten.

Further, as recited in claim 1, each ingress data port receives data from its corresponding first processor. This is also not taught by Scholten. Col. 7 lines 47-49 of Scholten (identified by the Final Office Action) describe:

> The plurality of transmit data FIFOs 310 receive data from one of the plurality of the ingress data processors 314, each of which is coupled to a particular input port 303. The ingress data processors 314 receives data from the corresponding input port 303 and formats the data into one or more data packets, wherein each data packet includes at least a destination identifier portion and data portion. (Scholten: col. 7 lines 45-47)

As is evident from the above, in Scholten, the ingress data processors 314 receive data from the corresponding input ports 303 – this is however not what is recited in claim 1. In claim 1, each data port receives data from its corresponding first processor – not the processor receiving data from the port, as described in Scholten. The input ports 303 in Scholten do not receive data from the corresponding processor. Accordingly, the structure described in the cited portion of Scholten is different from the structure recited in claim 1 wherein each ingress data port (not the first processor) is adapted to receive an input data stream from its corresponding first processor. Applicant thus submits that this feature of claim 1 is not taught or suggested by Scholten.

In disagreeing with reasons for patentability related to the circuit structure articulated by the Applicant in a response to the Final Office Action, the Advisory Action asserts:

> Applicant further argues that the first processors and the aggregation module cannot be considered in isolation. However, the claim language does not offer any such functionality. (Advisory Action)

As discussed above, Applicant submits that claim 1 clearly recites a plurality of ingress data ports, each said ingress data port coupled to a corresponding first processor and adapted to receive an input data stream from the corresponding first processor, an aggregation module coupled to said plurality of ingress data ports and configured to receive the plurality of input data streams from the first processors using the plurality of ingress data ports, a memory coupled to said aggregation module, and an output data port coupled to said aggregation module, said output data port adapted to output the aggregated data stream to the second processor. Accordingly, Applicant submits that the specific circuit structure is recited in claim 1.

The Advisory Action further asserts

> Further, Scholten's ingress data processors are part of one circuit which is of Fig. 2, 204A. Applicant argues that each ingress data port does not receive the input data stream from the first processor. However, examiner disagrees. Scholten teaches Transmit FIFOs receive data from ingress data processors which than send data to aggregation module. (Advisory Action)

Firstly, the Advisory Action fails to identify what in Scholten corresponds to the aggregation module recited in claim 1. In absence of an aggregation module, the circuit structure recited in claim 1 is not shown. Further, as described in col. 7 lines 47-49 in Scholten, the plurality of transmit data FIFOs 310 receive data from one of the plurality of the ingress data processors 314. It appears from this description that the FIFOs receive data from a single ingress data processor 314 one at a time, which seems to imply that the FIFOs receive the data from the ingress data processors over a single connection. This seems to be further confirmed by Fig. 3 of Scholten which shows a single line connection between ingress data processors 314 and transmit data FIFOs 310. This is different from the circuit structure recited in claim 1.

Applicant thus submits that even if Maher and Scholten were combined as suggested by the Final Office Action (even though there appears to be no motivation for the combination), the resultant combination would not teach or suggest the circuit recited in claim 1. Applicant thus submits that claim 1 is allowable over a combination of Maher and Scholten.

In light of the above, Applicant thus submits that claim 1 is patentable over a combination of Maher and Scholten.

Applicant further submits that dependent claims 2-15 that depend either directly or indirectly from claim 1 are also not rendered obvious by a combination of Maher and Scholten for at least a similar rationale as discussed above for claim 1. Applicant submits that the dependent claims are also patentable for additional reasons.

Claims 17 and 18

Claims 17 and 18 have been amended to depend from claim 1. Applicant submits that claims 17 and 18 are patentable over a combination of Maher and Scholten for at least a similar rationale as discussed above for claim 1.

Further, claim 17 recites that the aggregation module is implemented by a programmable device. Applicant submits that Maher and Scholten in combination do not teach this feature. Applicant would like to note here that, while the concept of a programmable device is known, the specific invention recited in claim 17 is of the aggregation module being implemented by a programmable device. Applicant submits that this is not taught or suggested by the references.

Claims 20-30

Applicant submits that claim 20 is not rendered obvious by a combination of Scholten and Maher and has amended claim 20 to further emphasize the inventive features. For example, Applicant's claim 20 recites:

> 20. A circuit for aggregating an input data stream from a first processor into an aggregated data stream for a second processor, said circuit comprising:
>
> a first data link adapted to receive the input data stream from the first processor, the ***first data link having a first bandwidth***, the input data stream formed of ingress data packets, each ingress data packet including priority factors coded therein;
>
> an aggregation module coupled to the first data link and adapted to receive the input data stream from the first processor via the first data link, said aggregation module adapted to analyze and selectively recombine the ingress data packets in response to the priority factors so as to generate an aggregated data;
>
> . . .
>
> a second data link coupled to said aggregation module, ***the second data link having a second bandwidth smaller than the first bandwidth***, said second data link adapted to output the aggregated data stream from the aggregation module to the second processor. (Applicant's claim 20, in part, emphasis added)

As specifically recited above, the aggregation module receives data from a first

processor via a first data link and a second data link is used to output the aggregated data stream from the aggregate module to the second processor. Further claim 20 specifically recites that the second data link has a bandwidth (the "second bandwidth") that is smaller than the bandwidth ("first bandwidth") of the first data link. Accordingly, as recited in claim 20, the bandwidth of the link used to output data from the aggregate module is smaller than the bandwidth of the link over which data is received by the aggregate module. Applicant submits that at least this feature recited in claim 20 is not rendered obvious by a combination of Maher and Scholten.

The Final Office Action acknowledges that Maher does not teach generating an aggregated data stream for a second data link having a second bandwidth smaller than the first bandwidth of a first data link where an ingress data port receives the input data stream from a first processor via the first data link and an output data port coupled to the aggregation module is adapted to output the aggregated data stream to the second processor (Final Office Action: page 9). The Final Office Action however alleges that this feature of claim 20 is taught by Scholten at col. 3 lines 47-55, Fig. 3 references 314 and 316, col. 1 lines 53-57, and col. 8 lines 38-50. Applicant respectfully disagrees.

Applicant submits that the various sections of Scholten cited by the Final Office Action fail to cure the deficiencies of Maher. For example, col. 3 lines 47-55 of Scholten describe that an aggregation module 102 (depicted in Fig. 1 of Scholten) receives ***lower*** bandwidth data packets from the plurality of input-output ports and outputs a ***higher*** bandwidth data signal for transmission via the high capacity network 104. Applicant however submits that this is completely different (and opposite) from what is claimed in claim 20. As recited in claim 20, the bandwidth of the second data link used to output the aggregated data stream from the aggregation module to the second processor is smaller than the first bandwidth of the first data link over which the input data stream is received by the ingress port from the first processor -- in this manner data streams are aggregated from a higher bandwidth data link to a lower bandwidth data link. In other words, in claim 1, the bandwidth of the link used to output data from the aggregate module is smaller than the bandwidth of the link over which data is received by the aggregate module. On the contrary, in Scholten col. 3 lines 47-55, module 102 receives ***lower***

bandwidth data packets from the plurality of input-output ports and outputs a ***higher*** bandwidth data signal. The invention recited in claim 20 aggregates data streams from a higher bandwidth data link to a lower bandwidth data link – whereas in Scholten, the data packets are aggregated from lower bandwidth data packets received from the plurality of input-output ports into a higher bandwidth data signal.

The description (pointed out by Examiner in the "Response to Arguments" section) in Scholten that:

> . . . the sum of the aggregated bandwidths of the data provided by the plurality of input-output ports 101, is less than or equal to the 10 GBPS data rate of the PSTN. (Scholten: col. 3 lines 52-55)

further emphasizes Applicant's arguments made above. This clearly shows that the bandwidths of data received by the aggregation module in Scholten are lower than the bandwidth on network 104 (PSTN). This shows that in Scholten the aggregation module 102 receives lower bandwidth data packets from the plurality of input-output ports and outputs a higher bandwidth data signal for transmission via the high capacity network 104 -- this is different from what is recited in claim 20.

The other sections of Scholten cited by the Final Office Action also fail to disclose the bandwidth features recited in claim 20. References 314 and 316 in Fig. 3 of Scholten point to ingress and egress data processors respectively with ports 303 and 315 coupled to the processors. With respect to Fig. 3 in Scholten, Examiner has not clearly articulated which data links in Fig. 3 of Scholten correspond to the first data link and the second data link recited in claim 20. Further, the Final Office Action fails to show which component in Fig. 3 of Scholten corresponds to the aggregation module as recited in claim 20. Due to the above and as best understood by the Applicant, Fig. 3 of Scholten fails to show that a bandwidth of a second data link used to output the aggregated data stream from the aggregation module to the second processor is smaller than the first bandwidth of the first data link over which the input data stream is received by the ingress port, as recited in claim 20. Accordingly, Applicant submits that claim 20 is not taught by Fig. 3 of Scholten.

Applicant further submits that, col. 8 lines 38-50 of Scholten also merely provide

description related to the input and output ports depicted in Fig. 3. Further, col. 1 lines 53-57 generally describe the advantages of providing fractional portions of high bandwidth capacity links. Applicant submits that, as discussed above for Fig. 3 of Scholten, these portions of Scholten also fail to teach the specific features recited in claim 20.

The Advisory Action asserts:

> Applicant argues that Scholten does not teach second bandwidth is smaller than the first bandwidth. However, examiner disagrees. Scholten teaches sum of the aggregated bandwidths of data provided by the plurality of ingress ports is less than the data rate of the network 104. Fig, 3, 314 corresponds to ingress data processors which form the first data link and Fig. 3, 316 corresponds to egress data processors which form the second data link. (Advisory Action, emphasis added)

Applicant submits that the above assertion actually provides support for and emphasizes the Applicant's reasoning discussed above. The fact that Scholten teaches that the sum of the aggregated bandwidths of data provided by the plurality of ingress ports is less than the data rate of the signal output to network 104 shows that in Scholten the bandwidth of the output link (to network 104) is greater than the bandwidth of the input links – this is completely different from claim 20 wherein the bandwidth of the output link (from the aggregate module) is smaller than the bandwidth of the input link.

Applicant thus submits that the deficiencies of Maher are not cured by Scholten. Applicant thus submits that even if Maher and Scholten were combined as suggested by the Final Office Action (even though there appears to be no motivation for the combination), the resultant combination would not teach or suggest the circuit recited in claim 20. Applicant thus submits that claim 20 is allowable over a combination of Maher and Scholten.

Applicant further submits that the dependent claims 21-30 that depend either directly or indirectly from claim 20 are also not rendered obvious by a combination of Maher and Scholten for at least a similar rationale discussed above for claim 20. Applicant submits that the dependent claims are patentable for additional reasons.

Claims 32-44

Applicant submits that claim 32 is not taught or suggested by Maher, or Scholten, considered individually or in combination. Claim 32 specifically recites in part:

> storing an analyzed data packet in a memory;
>
> generating a packet descriptor for the analyzed ingress data packet, the packet descriptor containing a reference to a memory location of its analyzed data packet stored in the memory;
>
> placing the packet descriptor in a priority queue corresponding to the priority class of the data packet;
>
> arbitrating and selecting a packet descriptor from among the priority queues using selection logic implementing a queue scheme;
>
> reading a data packet corresponding to the selected packet descriptor from the memory; (Applicant's claim 32, in part, emphasis added)

As shown above, claim 32 specifically recites a method of aggregating using a packet descriptor. Claim 32 specifically recites that the packet descriptor contains a reference to a memory location of the analyzed packet stored in the memory. It should further be noted that, as recited in claim 32, the packet descriptor is generated for an analyzed ingress data packet and is thus separate from and not part of the packet itself. Claim 32 further recites that the packet descriptor is placed in a priority queue corresponding to the priority class of the data packet. Further, a data packet corresponding to the selected packet descriptor is read from the memory and the data packets read from the memory are sent to the second processor as an aggregated data stream. Applicant submits that the concept of aggregating input data streams using a packet descriptor, as recited in claim 32, is not taught or suggested by Maher or Scholten, considered individually or in combination.

The Final Office Action asserts that the feature of generating a packet descriptor is disclosed by Maher in col. 9 lines 32-36 and placing of the packet descriptor in a priority queue is taught in col. 10 lines 58-67. Further, the Final Office Action alleges that the features of arbitrating and selecting using a packet descriptor is disclosed in Maher in col. 9 lines 47-51

and reading a data packet corresponding to the selected packet descriptor from the memory is disclosed by Maher in col. 9 lines 47-51. Applicant respectfully disagrees.

In col. 9 lines 32-36 Maher describes:

> Payload analyzer 110 processes blocks of data from multiple data packets each belonging to a unique traffic flow having an associated session id. In the preferred embodiment of the present invention, payload analyzer 110 processes 64 byte blocks of 64 different data packets from unique traffic flows simultaneously. Each of the 64 byte blocks of the 64 different data flows represents a single context for the payload analyzer. (Maher: col. 9 lines 26-32, emphasis added)

Accordingly, as best understood, a *context*, as used in Maher, is a 64 byte block of a packet belonging to a particular traffic flow. Since the context is a piece of a packet, unlike the packet descriptor recited in claim 32, it is not generated from analyzing an ingress data packet.

Further, since the context described in Maher is a part of the packet itself, it does not contain a reference to a memory location of the analyzed packet stored in the memory, as recited in claim 32.

Further, as recited in claim 32, the arbitrating and selecting is done using the packet descriptors. There appears to be no such teaching in Maher. In Maher, the processing seems to be done using the packets or portions of the packet.

In the "Response to Arguments" section of the Final Office Action, the Examiner states that the context represents the particular flow of packets and their memory location in the queue engine 302 and that this is generating the packet descriptor for packets in memory. Applicant submits, as described above, that the context is actually a piece of a packet and is thus not generated in the same manner that the packet descriptor is generated as recited in claim 32. Further, there appears to be no teaching in Maher that the context comprises a reference to a memory location of the analyzed data packet, as recited in claim 32.

The Advisory Action asserts

> Applicant argues that Maher does not teach generating a packet descriptor which contains a reference to a memory location of its analyzed data packet stores in the memory. However, examiner disagrees. Context is used to load packets in and out of buffer as taught by Maher in Col. 9. lines 63-66 therefore context is used as a reference to memory location of data

> packets in memory. Applicant argues that Maher does not teach arbitrating and selecting a packet descriptor from among the priority queues. However, examiner disagrees. Maher teaches using context which are packet descriptors to retriever required block of information from the memory. (Advisory Action)

Applicant submits that col. 9 lines 63-66 of Maher do not teach that the context is used to load packets in and out of a buffer as asserted by the Advisory Action. On the contrary, this section of Maher describes that the context is loaded into one of the buffers in context buffers 362 until it is retrieved by scheduler 364. Accordingly, in Maher as described, the context, which is a part of the packet, is itself loaded into the buffer – the context is not used to load a separate packet. Applicant submits even this section does not teach anything about a packet descriptor, as recited in claim 32, that contains a reference to a memory location of the analyzed packet stored in the memory Applicant subsequently submits that the processing done using a packet descriptor, as recited in claim 32, is also not taught by Maher.

In light of the above, Applicant submits that the concepts of a packet descriptor and its use for aggregating data streams, as recited in claim 32, are not taught or suggested by Maher.

Applicant further submits that the deficiencies of Maher are not cured by Scholten. As best understood, Scholten does not teach a packet descriptor and its use for aggregating data streams as recited in claim 32. Applicant thus submits that even if Maher and Scholten were combined as suggested by the Final Office Action (even though there appears to be no motivation for the combination), the resultant combination would not teach or suggest the features recited in claim 32. Applicant thus submits that claim 32 is not rendered obvious by a combination of Maher and Scholten.

Applicant further submits that the dependent claims 33-45 that depend either directly or indirectly from claim 32 are also not rendered obvious by a combination of Maher and Scholten for at least a similar rationale discussed above for claim 32. Applicant submits that the dependent claims are patentable for additional reasons.

Claim 46

Applicant submits that claim 46 is not rendered obvious by a combination of Maher and Scholten, and has further amended claim 46 to highlight the differences. Applicant's claim 46 recites:

> 46. A method for aggregating a plurality of input data streams from first processors into one data stream for a second processor, said method comprising:
>
> providing, for each first processor, an analyzer corresponding to the first processor, the analyzer being separate from the first processor and located in a communication path between the first processor and the second processor;
>
> receiving an input data stream from each of the first processors, each input data stream formed of ingress data packets, each ingress data packet including priority factors coded therein;
>
> generating an aggregated data stream by analyzing and combining the plurality of input data streams into one aggregated data stream in response to the priority factors, the priority factors including an indication of whether the ingress packet contains protocol data or not, wherein the generating comprises, for each first processor, receiving the input data stream from the first processor at an analyzer corresponding to the first processor, and analyzing the input data stream received from the first processor using the analyzer; and
>
> outputting the aggregated data stream to the second processor. (Applicant's claim 46, emphasis added)

As recited above, analyzer is provided for each first processor, the analyzer being separate from the first processor and located in a communication path between the first processor and the second processor. Claim 46 further recites that as part of generating the aggregated data stream, an analyzer corresponding to a first processor receives the input data stream from the first processor and analyzes the input data stream. Applicant submits that at least these features recited in claim 46 are not taught or suggested by Maher or Scholten.

The Final Office Action acknowledges that Maher fails to teach a first processor and second processor being used for sending and receiving data streams, each first processor having a corresponding analyzer, and analyzing the input data stream from the first processor using the corresponding analyzer (Final Office Action: pg. 13). The Final Office Action

however goes on to assert that these features are taught by Scholten at col. 5 lines 38-48. Applicant respectfully disagrees.

Col. 5 lines 38-48 of Scholten describe the link layer devices depicted in Fig. 2 of Scholten that are connected in a daisy-chain manner. Each link layer device has a data receiver for receiving data and a transmitter for outputting data. A link layer device is configured to divert data packets to virtual channels based upon destination identifiers in the data packets.

Applicant fails to see how this daisy-chaining of link layer devices teaches the analyzers-related features recited in claim 46. Even if a link layer device described in Scholten is considered as a first processor recited in claim 46, Scholten still fails to teach anything about an analyzer corresponding to each link layer device that performs analysis to generate an aggregated data stream. Applicant notes that as best understood, the data receiver of a link layer device is merely a means for receiving data and is not an analyzer as recited in claim 46. There appears to be no teaching in Scholten that the receiver performs analysis for purposes of aggregating data streams, as recited in claim 46.

Further, claim 46 as amended specifically recites that an analyzer is separate from its corresponding first processor and is located in a path between the first processor and the second processor. Applicant submits that such a set of analyzers is not disclosed by Scholten.

In the "Response to Arguments" section of the Final Office Action, the Examiner states that Scholten teaches forwarding packets according to a unique destination identifier associated with a packet and that this is analyzing the packet from the input data stream. Applicant would like to point out that claim 46 recites a specific structure of each first processor has a corresponding analyzer that analyzes the input data stream received from the first processor. Applicant submits that this structure, as recited in claim 46, is not taught by Scholten. The point raised by the Examiner that the packet is analyzed in Scholten does not imply that the structure recited in claim 46 is taught by Scholten.

The Advisory Action asserts that

> Applicant argues that Scholten does not teach analyzing input data streams and each processor has an input analyzer. However, examiner disagrees. Scholten teaches the

> device diverts the packets based on a destination identifier. This is analyzing data packets based on destination identifier. (Advisory Action)

Applicant submits that claim 46 recites a specific structure of analyzers corresponding to first processors – not just the analysis of the data streams. Applicant submits that the specific structure recited in claim 46 is not taught by Scholten.

In light of the above, Applicant submits that the deficiencies of Maher are not cured by Scholten. Applicant thus submits that even if Maher and Scholten were combined as suggested by the Final Office Action (even though there appears to be no motivation for the combination), the resultant combination would not teach or suggest the features recited in claim 46. Applicant thus submits that claim 46 is not rendered obvious by a combination of Maher and Scholten.

Claim 47

Applicant's claim 47 recites:

> 47. A method for aggregating data packets, said method comprising:
>
> receiving an input data stream from a first processor via a first data link having a first bandwidth, the input data stream formed of ingress data packets, each ingress data packet including priority factors coded therein;
>
> generating an aggregated data stream by analyzing and selectively recombining the ingress data packets in response to the priority factors, the priority factors including an indication of whether the ingress packet contains protocol data or not; and
>
> outputting the aggregated data stream to a second processor via a second data link having a second bandwidth, wherein the first bandwidth is greater than the second bandwidth. (Applicant's claim 47, emphasis added)

Claim 47 thus specifically recites that the aggregated data stream is generated by analyzing and selectively recombining the ingress data packets and further that an input data stream is received from a first processor via a first data link having a first bandwidth that is greater than a second bandwidth of a second data link used to output the aggregated data stream to the second processor. Applicant submits that at least these features recited in claim 47 are not taught or suggested by Maher or Scholten, considered individually or in combination.

The Final Office Action acknowledges that Maher does not teach outputting the aggregated data stream to a second processor via a second data link having a second bandwidth that is smaller than a first bandwidth for receiving an input data stream from a first processor. The Final Office Action however asserts that this feature of claim 47 is taught by Scholten at col. 3 lines 47-55, Fig. 3 references 314 and 316, col. 1 lines 53-57, and col. 8 lines 38-50.

Applicant submits that these sections of Scholten do not teach the features recited in claim 47 related to the bandwidths for at least a similar rationale as discussed above for claim 20. Applicant thus submits that the deficiencies of Maher are not cured by Scholten. Applicant thus submits that even if Maher and Scholten were combined as suggested by the Final Office Action (even though there appears to be no motivation for the combination), the resultant combination does not teach or suggest the features recited in claim 47. Applicant thus submits that claim 47 is not rendered obvious by a combination of Maher and Scholten.

Examiner's response in the "Response to Arguments" section of the Final Office Action fails to mention anything about the bandwidths-related features, as recited in claim 47.

Claim 16

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Maher in view of Scholten and further in view of Manaka et al (U.S. Patent No. 6,421,352) (hereinafter "Manaka").

Claim 16 depends from claim 1 and is thus not rendered obvious by a combination of Maher and Scholten for at least the reasons discussed above for claim 1. Further, Applicant submits that the deficiencies of Maher and Scholten are not cured by Manaka, considered individually or in combination. Manaka has been cited for specific teachings and does not teach the features of claim 1 discussed above that make claim 1 patentable over Maher. Accordingly, even if Maher, Scholten, and Manaka were combined as suggested by the Final Office Action (even though there appears to be no motivation for the combination), the resultant combination would not render claim 16 obvious.

Claims 17 and 49

Claims 17 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maher in view of Scholten and further in view of Abbas et al. (U.S. Patent No. 6,810,046) (hereinafter "Abbas").

Claim 49 has been canceled without prejudice.

Claim 17 has been amended to depend from claim 1 and is thus allowable over a combination of Scholten and Maher for at least a similar rationale as discussed above for claim 1. Further, the deficiencies of Maher and Scholten are not cured by Abbas. Accordingly, even if Maher, Scholten, and Abbas were combined as suggested by the Final Office Action (even though there appears to be no motivation for the combination), the resultant combination would not render claim 17 obvious.

Claims 19, 45, and 63

Claims 19, 45 and 63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maher in view of Scholten and further in view of Mackiewich et al (U.S. Patent No. 7,212,536) (hereinafter "Mackiewich").

Claim 63 has been cancelled without prejudice.

Applicant submits that claim 19, which depends from claim 18 which depends from claim 1, is not rendered obvious by a combination of Maher and Scholten for at least a similar rationale as discussed above for claims 1 and 18. Further, Applicant submits that the deficiencies of Maher and Scholten are not cured by Mackiewich. Mackiewich is cited by the Final Office Action for a very specific teaching and does not teach the features of claim 18 discussed above that make claim 18 patentable over a combination of Maher and Scholten. Accordingly, even if Maher, Scholten, and Mackiewich were combined as suggested by the Final Office Action (even though there appears to be no motivation for the combination), the resultant combination would not render claim 19 obvious.

Applicant submits that claim 45, which depends from claim 32, is not rendered obvious by a combination of Maher and Scholten for at least a similar rationale as discussed

above for claim 32. Further, Applicant submits that the deficiencies of Maher and Scholten are not cured by Mackiewich. Mackiewich is cited by the Final Office Action for a very specific teaching and does not teach the features of claim 32 discussed above that make claim 32 patentable over Maher. Accordingly, even if Maher, Scholten, and Mackiewich were combined as suggested by the Final Office Action (even though there appears to be no motivation for the combination), the resultant combination would not render claim 45 obvious.

Amendments to the Claims

Unless otherwise specified, amendments to the claims are made for purposes of clarity, and are not intended to alter the scope of the claims or limit any equivalents thereof. The amendments are supported by the Specification as filed and do not add new matter.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,

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